

High Precision CMOS Sensors: R&D Status and Plans

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Outline

- ▶ **Introductory remarks: important fabrication parameters**
- ▶ **Achieving a High Read-Out Speed**
- ▶ **Exploring new fabrication processes**
- ▶ **The Issue of Radiation Hardness**
- ▶ **Summary & Outlook**

CMOS Sensors: Principle and Advantages

► Principle of Operation:

- **p-type low-resistivity Si**

⇒ **only NMOS transistors allowed**

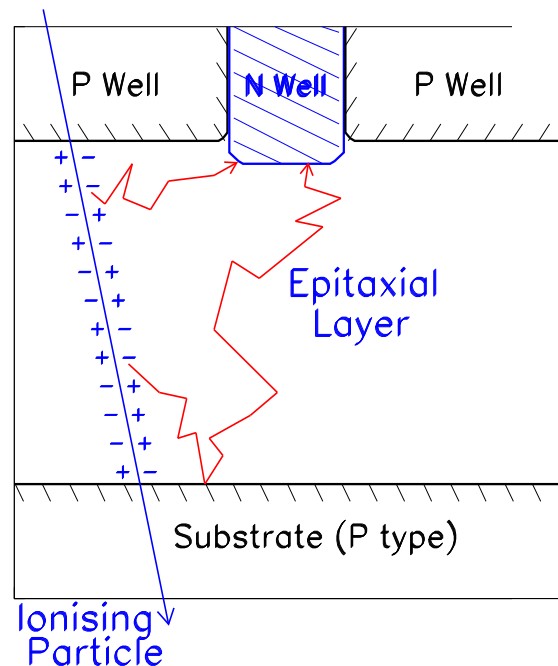
↷ **signal charge created in epitaxial layer**

(low doping) : $Q \sim 80 \text{ e-h} / \mu\text{m}$

↷ **charge collected by diode (n-well)**

↷ **excess carriers propagate to diode with help of reflection on boundaries**

with p-well and substrate (high doping)



► Important fabrication parameters:

- **feature size**
- **epitaxial layer characteristics: thickness, doping profile,**
if no epitaxial layer → low substrate doping
- **nb of metal layers**
- **transistor polarisation voltages**
- **leakage current**
- **insulator composition**
- **etc.**

► Exploring fabrication processes is a permanent activity ...

Advantages and established Tracking potential

► Advantages:

- signal processing μ circuits integrated on sensor substrate:
inside pixels (NMOS transistors, capacitors) & on chip periphery
 \hookrightarrow System-on-Chip (SoC)
- sensitive volume (\sim epitaxial layer) is $\sim 10 \mu m$ thick
 \hookrightarrow sensors may be thinned down to $< 20 \mu m$
- standard, massive production, fabrication technology
 \hookrightarrow cheap, fast turn-over
- spatial resolution and material budget as attractive as with CCD
 BUT higher read-out speed and radiation tolerance

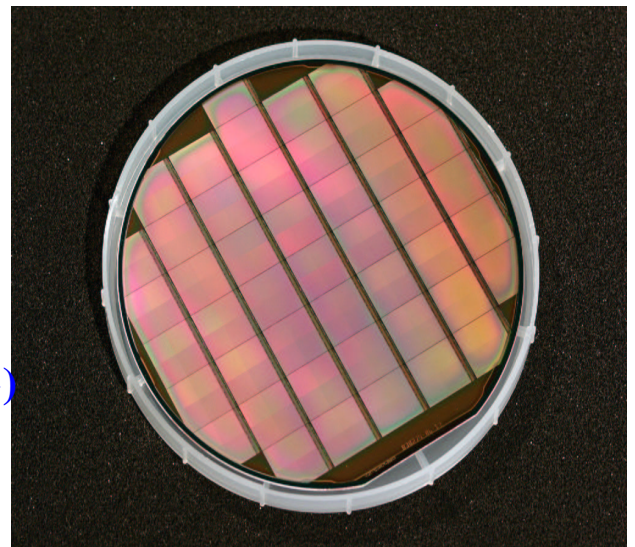
► CMOS sensors designed in Strasbourg since 1999

- 9 prototypes (called MIMOSA) designed (2 with Saclay)
 \hookrightarrow 8 chips fabricated out of which 6 tested
- Adequacy for particle tracking demonstrated:
 $\hookrightarrow \epsilon_{det} > 99\%, \sigma_{sp} \sim 1.5 \mu m$
- Developed for future Vertex Detectors (e.g. Linear Collider)
 and for biomedical imaging and therapy, dosimetry, etc.

MIMOSA-5: 1st real scale prototype

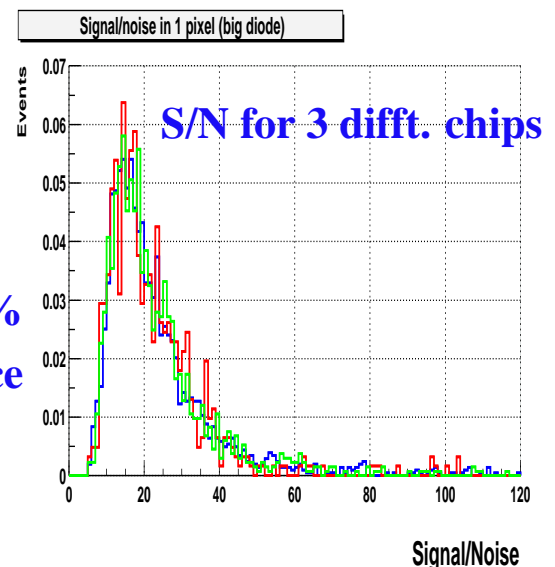
► Main characteristics:

- 19.4 x 17.4 mm² wide chips made of ~ 1 million pixels (17 μm pitch)
- each chip = 4 arrays read out in //
each array = 512x512 pixels
- fab. process: AMS 0.6 μm (6" wafers \longrightarrow)
- 3 wafers thinned down to 120 μm
(some chips thinned to 15 μm !)



► 4 chips exposed to 120 GeV/c π^- at CERN-SPS:

- Noise ~ 20 e⁻ ENC
- S/N ~ 20 (seed pixel - see figure)
- detection efficiency ~ 99 %
- single point resolution ~ 2 μm
- gain dispersion over chip surface ~ 0.3 %
- very homogeneous perfo. over chip surface
- very small dispersion from chip to chip



► Application to STAR Vertex Detector Upgrade:

- performances close to specifications of STAR Vx Det. upgrade (2006)
- optimised chip (MIMOSTAR-1) being designed:
 - ★ r.o. time = 4-8 ms
 - ★ spatial resolution ~ 3 μm (30 μm pitch)
 - ★ chip thickness ~ 50 μm
 - ★ 2 layers, i.e. ~ 1000 cm² to cover

Achieving high read-out speed (1)

- ▶ **High read-out speed requires massively // signal treatment**
 - ↪ **detector plane subdivided into sub-arrays**
(serial treatment of the pixels inside each sub-array)
 - ↪ **watch the data flow !**

- ▶ **Number of pixels per sub-array (N_{pix}) ?**

- N_{pix} is limited by max $t_{R.O.}$ allowed → upper limit
and by Q coll. time → low limit
- charge coll. time $\lesssim 100$ ns (depends on sensitive volume)
⇒ $t_{R.O.} \gg 1 \mu s$ mandatory
- signal treatment inside pixel:

$$f_{st} \gtrsim \frac{f_{clock}}{N_{clock}} \sim \frac{50 \cdot 10^6}{5} \sim 10 \text{ MHz}$$

↪ $N_{pix}/\text{sub-array}$:

$$t_{R.O.} = \frac{N_{pix}}{f_{st}} \rightarrow 100 \text{ pixels for } 10 \mu s$$

Achieving high read-out speed (2)

► Number of sub-arrays to treat in parallel ?

- detector surface (S_D) subdivided in N_{sa} subarrays

$$N_{sa} = \frac{S_D}{100 p^2} \rightarrow N_{sa}/\text{cm}^2 = 10^6/p^2 \text{ (p in } \mu\text{m)}$$

$$p = 20 \mu\text{m} \rightarrow 2500 \text{ sub-arrays / cm}^2$$

$$p = 40 \mu\text{m} \rightarrow 625 \text{ sub-arrays / cm}^2$$

► Choice of pixel pitch according to:

- impact parameter resolution
(depends also on material budget and lever arm)
- double hit resolution
(depends also on sensitive volume \rightarrow cluster size ,
 T_{op} , tracking performances)
- occupancy
(depends also on $t_{R.O.}$)
- signal charge collection efficiency
(depends also on sensitive volume)

Achieving high read-out speed (3)

► Conclusion:

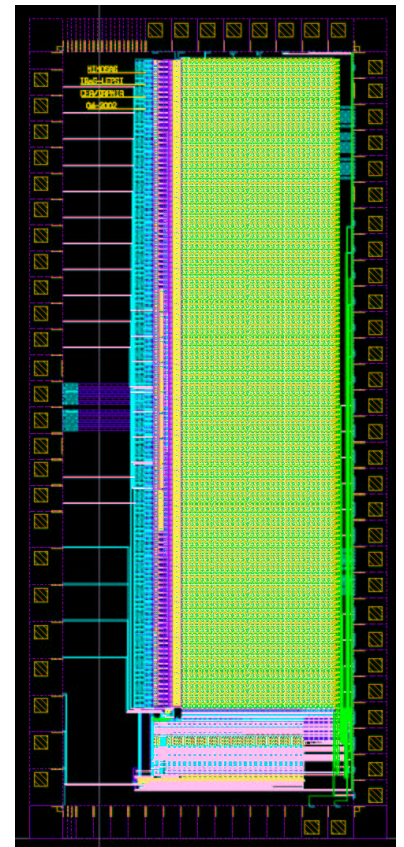
- Monte Carlo simulations:
impact parameter resolution, double hit resolution, occupancy
- fabrication process exploration:
sensitive vol., signal charge coll. eff., influence of $T_{op} \rightarrow S/N$
- exploration of signal collection & treatment architectures:
 $S/N, f_{clock}, f_{st}, P_{diss}$

Achieving high read-out speed (4)

- ▶ Chips organised in columns read out in parallel
- ▶ Main difficulty: data flow ($\sim 1 \text{ Tbit/s/cm}^2$)
 - ↪ very effective integrated signal processing mandatory

- ▶ 1st sensor with sparsification integrated / substrate fab. in 2002:
 - ◇ made of 30 columns of 128 pixels ($20 \mu\text{m}$ pitch)
 - ◇ column read-out time $\sim 25 \mu\text{s}$
 - ◇ pre-amplification (x5.5) and CDS integrated inside each pixel (29 T and 3 capa / pixel)
 - ◇ discriminator integrated on chip periphery (1 discri. per column; design in Saclay)

- ↪ Main test results (^{55}Fe source):
 - ★ individual pixel works fine:
 - 5.9 keV X-Rays observed; $N \sim 15 \text{ e}^- \text{ ENC}$
 - ★ comparators work fine
 - ★ BUT pixel to pixel signal dispersion is too large



Achieving high read-out speed (5)

- ▶ 2 new prototypes were designed in 2003
- ▶ MIMOSA-7:
 - AMS 0.35 μm fab. process without epitaxial layer
 - test of new charge coll. system, based on low noise preamplifier integrated inside n-well (PhotoFET)
 - ↪ back from foundry; tests in preparation → results in Autumn
- ▶ MIMOSA-8 (with Saclay):
 - TSMC 0.25 μm fab. process with 8 μm epitaxial layer and 2 transistor polarisations
 - test of high gain (15 ?) low noise preamplifier inside pixel
 - ↪ back from foundry \lesssim March
tests in preparation → results end 2004 ?

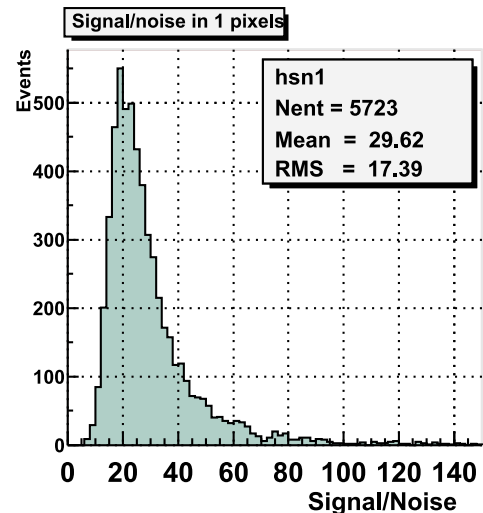
Exploration of non-standard technologies

► Processes without epitaxial layer but with low doping substrate

- MIMOSA-4 fab. in AMS $0.35\mu m$ no-epi.

- Tests with $120\text{ GeV}/c\ \pi^-$ at CERN-SPS:

- ★ $S/N \sim 30$ (large signal charge)
- ★ detection efficiency $\gtrsim 99.5\%$
- ★ single point resolution $\sim 2.5\mu m$
($20\mu m$ pitch)



- SUCCESSOR-2 fab. in same process but with $40\mu m$ pitch

- ★ detection efficiency $\gtrsim 99.9\%$
- ★ single point resolution $\sim 5\mu m$

↪ Low doping substrate offers long e^- life time

⇒ Technology without epitaxial layer is very promising ...

↪ $40\mu m$ pitch works well

► Processes with thick epitaxial layer (for imaging) and low leakage current (\Rightarrow low noise at T_{room})

- MIMOSA-9 designed in AMS $0.35\mu m$ OPTO process

(perhaps $\sim 20\mu m$ epitaxial layer ...)

↪ back from foundry in April-May \Rightarrow test results for Summer

The issue of radiation hardness

► Bulk damage:

- Tests of MIMOSA-1 and -2:

Q(cluster) loss for $\lesssim 10^{12} n_{eq}/cm^2$ (and modest noise increase)

↪ ϵ_{det} loss of a few %

- Rad. tol. is process dependent \Rightarrow need more measurements,
esp. from other fab. processes (e.g. no-epi)

↪ Room for improvement ? \rightarrow explore recovering procedures (vs t, T)

► Ionising radiation:

- Few 100 kRads demonstrated to be OK

- Rad. tol. depends strongly on fabrication details

↪ limit not yet found for no-epi fab. process (AMS-0.35 μm)

- Understanding of phenomena and parameters involved relies on
exploration of fab. processes & on MC simulations (ISE-TCAD)

↪ Work under way (also an issue for bio-medical applications)

Summary & Outlook

► Summary of 2003:

- Tests of reticle size chips MIMOSA-5: excellent homogeneity
 ↪ started design of MIMOSTAR-1
- Tests of no-epi proto.: excellent ϵ_{det} & $\sigma_{sp} - 40 \mu m$ pitch works
- Tests of 1st fast (Col. Paral.) chip (M-6):
 individual pixel and dicri. OK but too large signal dispersion
- Radiation tolerance investigations
- Design of 2 other Col. Paral. chips (M-7 & -8)
- Design of 1st prototype in OPTO technology (M-9)

► Plans for 2004:

- Fabricate & test MIMOSTAR-1 (and proto-ladder with M-5)
 ↪ start design of MIMOSTAR-2
- Pursue thinning tests with MIMOSA-5
- Test Col. Paral. prototypes MIMOSA-7 & -8
 ↪ start design of next generation
- Test OPTO prototype MIMOSA-9
- Pursue studies of radiation tolerance